UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/844,481 | 04/27/2001 | Yasuhiko Onishi | FUJI:185 | 9134 |

7590 04/03/2003

ROSSI & ASSOCIATES
P.O. Box 826
Ashburn, VA 20146-0826

| EXAMINER |
|---|
| LANDAU, MATTHEW C |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 04/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/844,481 | Applicant(s) ONISHI ET AL. | |
|---|---|---|---|
| | Examin r Matthew Landau | Art Unit 2815 | |

*-- The MAILING DATE of this communication appears on the cov r sh et with th corr spondence addr ss --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,4-17,31 and 33* is/are pending in the application.

4a) Of the above claim(s) *5,8-13,15-17 and 33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,14 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Election/Restrictions*

1. Claims 5, 8-13, 15-17, and 33 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 7.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

overcome 3. Claims 6 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Coe.

In regards to claim 6 and 7, Figures 1 and 2 of Coe disclose a semiconductor chip; two main electrodes (23 and 24) on one major surface of the semiconductor chip; and an alternating conductivity type layer 3 between the main electrodes: wherein the alternating conductivity type layer comprises first semiconductor regions 11 of a first conductivity type and second semiconductor regions 12 of a second conductivity type: where the first semiconductor regions and the second semiconductor regions are alternately arranged; wherein the alternating

conductivity type layer comprises a closed loop surrounding one of the main electrodes (23); wherein the alternating conductivity type layer comprises at least one straight section and at least one curved section; and wherein the first semiconductor regions and the second semiconductor regions and the second semiconductor regions are arranged alternately at a first pitch in the straight section, and the first semiconductor regions and the second semiconductor regions are arranged alternately at a second pitch in the curved sections. Note Coe discloses only one pitch for the alternating conductivity type layer therefore the pitch in the straight section (first pitch) is the same as the pitch in the curved sections (second pitch).

4. Claims 1, 2, 4-7, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Magri' et al. (US Pat. 6,492,691, hereinafter Magri).

In regards to claim 1, Figures 5-8 of Magri disclose a semiconductor chip; two main electrodes 36 on one major surface of the semiconductor chip; and an alternating conductivity type layer (33/34) between the main electrodes: wherein the alternating conductivity type layer comprises first semiconductor regions 33 of a first conductivity type and second semiconductor regions 34 of a second conductivity type; wherein the first semiconductor regions and the second semiconductor regions are alternately arranged in a surface portion of the major surface; wherein the alternating conductivity type layer comprises a closed loop formed by the first and second semiconductor regions alternately arranged along the direction of the closed loop and surrounding one of the main electrodes; and wherein the alternating conductivity type layer comprises at least one straight section and at least one curved section.

In regards to claims 2, 6, and 7, Figures 5-8 of Magri disclose a semiconductor chip; two main electrodes 36 on one major surface of the semiconductor chip; and an alternating conductivity type layer 32 between the main electrodes: wherein the alternating conductivity type layer comprises first semiconductor regions 33 of a first conductivity type and second semiconductor regions 34 of a second conductivity type; wherein the first semiconductor regions and the second semiconductor regions are alternately arranged; wherein the alternating conductivity type layer comprises a closed loop surrounding one of the main electrodes; wherein the alternating conductivity type layer comprises first sections, wherein the first semiconductor regions and the second semiconductor regions are arranged alternately at a first pitch, and second sections, wherein the first semiconductor regions and the second semiconductor regions are arranged alternately at a second pitch different from the first pitch. The different pitches can be seen in Figure 6 wherein the top straight section has one pitch and the curved portion has another pitch.

In regards to claims 4 and 5, Figure 5 of Magri discloses the alternating conductivity type layer 32 comprises at least four straight sections and at least 4 curved sections.

In regards to claim 14, Figure 5 of Magri discloses a plurality of closed loops, each including the alternating conductivity type layers.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaguchi et al. (US Pat 6,297,534, hereinafter Kawaguchi) in view of Bhatnagar et al. (US Pat. 5,710,455, hereinafter Bhatnagar).

In regards to claim 1, Figure 1 of Kawaguchi discloses a semiconductor chip; two main electrodes (9 and 10) on one major surface of the semiconductor chip; and an alternating conductivity type layer (4/5) between the main electrodes; wherein the alternating conductivity type layer comprises first semiconductor regions 4 of a first conductivity type and second semiconductor regions 5 of a second conductivity type; wherein the first semiconductor regions and the second semiconductor regions are alternately arranged in a surface portion of the major surface. The difference between Kawaguchi and the claimed invention is the alternating conductivity type layer comprises a closed loop formed by the first and second semiconductor regions alternately arranged along the direction of the closed loop and surrounding one of the main electrodes, and wherein the alternating conductivity type layer comprises at least one straight section and at least one curved section. Figures 1 and 2 of Bhatnagar disclose a lateral semiconductor device with a semiconductor region between two main electrodes (15 and 17); wherein the semiconductor region forms a closed loop surrounding one of the main electrodes (17), and wherein the semiconductor region comprises at least one straight section and one

curved section. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kawaguchi by using the closed loop configuration of Bhatnagar for the purpose of eliminating the need for any special edge termination outside the device (column 6, lines 1-9).

In regards to claim 31, Figure 1 of Kawaguchi the lateral semiconductor device comprises a MOSFET (column 5, lines 51-55). It is further obvious in the invention of Kawaguchi and Bhatnagar to use the configuration of Bhatnagar wherein the high potential main electrode 17 is inside the closed loop and the low potential main electrode 15 is outside the closed loop (column 6, lines 1-9) for the purpose of containing the high voltage drain region inside the device.

***Allowable Subject Matter***

7. The indicated allowability of claim 2 is withdrawn in view of the newly discovered reference(s) to Magri.

The allowability of claims 6 and 7 is withdrawn in view on the new grounds of rejection.

***Response to Arguments***

8. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (703) 305-4396.

The examiner can normally be reached on 8:00 AM-4: 30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Matthew C. Landau

Examiner

March 30, 2003